Dkt: 303.326US1

## Specification

The applicant thanks the Examiner for the helpful suggestion regarding claim 35. The applicant made several changes to the specification in the amendment filed on July 15, 1999. If the Examiner would like further changes to be made to the specification the applicant requests that the Examiner specifically point out the changes to be made. The applicant respectfully submits that the specification complies with 35 U.S.C. §112.

## Rejections under 35 U.S.C. §103

Claims 1 and 8 were rejected under 35 USC § 103(a) as being unpatentable over Chen et al. (U.S. Patent No. 5,714,766, Chen) in view of Oyama (JP Patent No. 3-222,367). The applicant respectfully traverses.

Chen issued on February 3, 1998, which is after the filing date of the present application. The applicant does not admit that Chen is prior art, and reserves the right to swear behind Chen at a later date.

Claim 1 recites a transistor comprising, among other elements, a semiconductor surface layer formed on an underlying insulating portion, and an electrically interconnected gate formed of a silicon carbide material.

Oyama discloses a transistor with a silicon carbide gate, and discloses that silicon carbide gates are useful in some transistors. Chen discloses a memory cell in a silicon on insulator (SOI) substrate.

There must be a showing of a "teaching or motivation to combine prior art references" to support a rejection under section 103 and "the showing must be clear and particular." *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). However, there is no motivation in either Oyama or Chen for the combination thereof.

The Examiner states that Chen discloses a floating gate 34. The applicant respectfully traverses. The element 34 in Chen is a plurality of nanocrystals 34 that each store electrons or holes. Column 3, lines 64-66. The nanocrystals 34 may be silicon carbide and are each "physically confined in three dimensions." Column 4, lines 10-18. The nanocrystals 34 are shown in Figures 8 and 9 as being spaced apart and surrounded by a barrier material 30 in the memory cell 128. The barrier material 30 is an insulator of silicon oxide. Column 4, line 53.

The nanocrystals 34 therefore do not comprise a gate because a gate is known to those skilled in the art as a continuous, electrically conductive structure that has the same potential across its volume. In contrast, each nanocrystal 34 may hold a separate potential different from the potential of others of the nanocrystals 34. Therefore the nanocrystals 34 do not comprise a floating gate, and do not represent a motivation to combine Oyama and Chen.

The applicant respectfully submits that there are no other disclosures in either Oyama or Chen that provide a clear and particular motivation for the combination thereof. The applicant respectfully submits that claims 1 and 8 are not disclosed or suggested by the combination of Oyama and Chen, and that claims 1 and 8 are in condition for allowance.

Claims 2-7, 9-15, and 22-36 were rejected under 35 USC § 103(a) as being unpatentable over Chen in view of Oyama, and further in view of Halvis et al. (U.S. Patent No. 5,369,040, Halvis) and Forbes (U.S. Patent No. 5,801,401). The applicant respectfully traverses.

Forbes issued on September 1, 1998, which is after the filing date of the present application. The applicant does not admit that Forbes is prior art, and reserves the right to swear behind Forbes at a later date.

Claims 2-7, 9, and 10 are dependent on claim 1. For the reasons stated above, and the limitations in the claims, the applicant respectfully submits that claims 2-7, 9, and 10 are not disclosed or suggested by the combination recited above, and that claims 2-7, 9, and 10 are in condition for allowance.

Regarding claims 11-15 and 22-36, neither Halvis nor Forbes provide a motivation for the combination that is missing in Chen and Oyama, or a motivation for the inclusion of Halvis and Forbes in the combination. The Examiner stated claims 11-15 were rejected per the rejection of claims 1-10. The applicant respectfully submits that there is no clear and particular motivation for the combination put forward by the Examiner, that claims 11-15 and 22-36 are not disclosed or suggested by the combination recited above, and that claims 11-15 and 22-36 are in condition for allowance.

Serial Number: 08/903,486 Filing Date: July 29, 1997

Title: SILICON CARBIDE GATE TRANSISTOR

## CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

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CERTIFICATE UNDER 37 CFR 1.10:

"Express Mail" mailing label number: EL431988231US

Date of Deposit: November 3, 1999

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Chris Hammond

Signature